Studies of molecular-beam epitaxy growth of GaAs on porous Si substrates

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GaAs has been grown on porous Si directly and on Si buffer layer–porous Si substrates by molecular-beam epitaxy. In the case of GaAs growth on porous Si, transmission electron microscopy (TEM) reveals that the dominant defects in GaAs layers grown on porous Si are microtwins and stacking faults, which originate from the GaAs/porous Si interface. GaAs is found to penetrate into the porous Si layers. By using a thin Si buffer layer (50 nm), GaAs penetration diminishes and the density of microtwins and stacking faults is largely reduced and localized at the GaAs/Si buffer interface. However, there is a high density of threading dislocations remaining. Both Si (100) aligned and four degree tilted substrates have been examined in this study. TEM results show no observable effect of the tilted substrates on the quality of the GaAs epitaxial layer.

I. INTRODUCTION

Because of the potential in integration of GaAs and Si circuits monolithically, the GaAs on Si technology has recently drawn a great deal of interest. However, the 4% mismatch between GaAs and Si lattice constants causes the generation of a large density of misfit dislocations. The problem is exacerbated by the large difference of the thermal expansion coefficients between GaAs and Si which results in a very large postgrowth tensile stress in the grown GaAs layers.

Several approaches, such as the use of strained-layer superlattice,[1] rapid thermal annealing,[2] and tilted substrates,[1] have been utilized to suppress the propagation of threading dislocations toward the GaAs active region. To date, however, the total defect density of the epitaxial layers grown on Si substrates is still much higher than that on GaAs substrates.

Recently, a possible approach for growing defect-free materials on lattice mismatched substrates has been suggested by Luryi and Suhir[3] in which a substrate having small seed pads of a lateral dimension about 10 nm is used. However, this small size of seed pads is extremely difficult to achieve if not impossible by present lithography techniques. Alternatively, porous Si substrates which have surface pads with dimensions ranging from 3 to 20 nm appear to be an ideal substrate with seed pads for epitaxial growth.

Based on this idea, lattice mismatched GaAs[4] and $CoSi_2$[5] films have been previously grown on porous Si showing good crystallinity and surface morphology. The dominant defects in the GaAs layers are found to be microtwins and stacking faults. In this study, a thin Si buffer layer is grown on top of porous Si substrates to examine its effects on defect structure. Tilted Si substrates as well as aligned (100) Si substrates are used to study their effects on the GaAs layer grown both directly on porous Si and on buffer layer–porous Si substrates.

II. EXPERIMENT

Porous Si is formed by anodizing single-crystalline Si substrates in HF electrolyte.[6] The porosity is determined by the anodizing current density, HF concentration, and substrate doping density. *P*-type Si (100) substrates with a resistivity of 0.02 Ω cm are first cleaned by repeatedly boiling in nitric acid and dipping in HF. Then, the porous Si layers are formed by anodizing the substrates in a 30% HF electrolyte. After anodization, a protective oxide layer is formed immediately in a H_2SO_4:H_2O_2:H_2O = 4:1:4 solution.

To grow the Si buffer layer, the substrate is loaded into the Si molecular-beam epitaxy (MBE) growth chamber. The protective oxide layer is removed by the Si beam self-cleaning method at 750 °C.[7] The Si buffer layer is grown at a growth rate of 3 nm/min. Then, the substrate is unloaded from the Si MBE chamber and another protective oxide layer is formed on the Si substrates.

Prior to GaAs growth, the substrate is dipped in 49% HF in N_2 ambient[8] to remove the protective oxide. No further high-temperature treatment except outgassing at 700 °C is performed on the substrates so as to prevent the collapse of the porous Si structure. GaAs epitaxial growth is performed by a two-step growth technique. The first layer is grown at 500 °C for 20 nm with 0.4 μm/h growth rate and the second layer is grown at 650 °C for 1-μm thickness with 1 μm/h growth rate.

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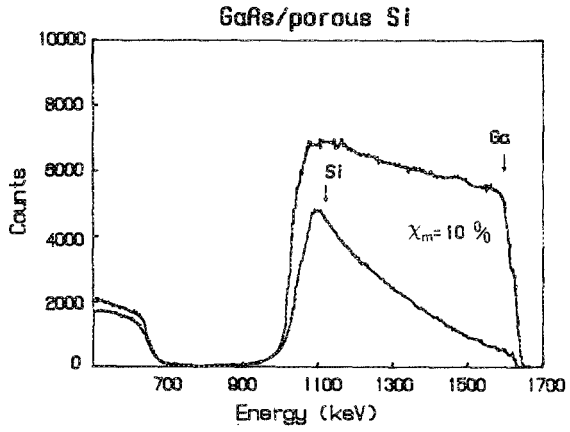

FIG. 1. (a) RBS of GaAs on porous Si (aligned substrate). (b) RBS of GaAs on single-crystalline Si (aligned substrate).

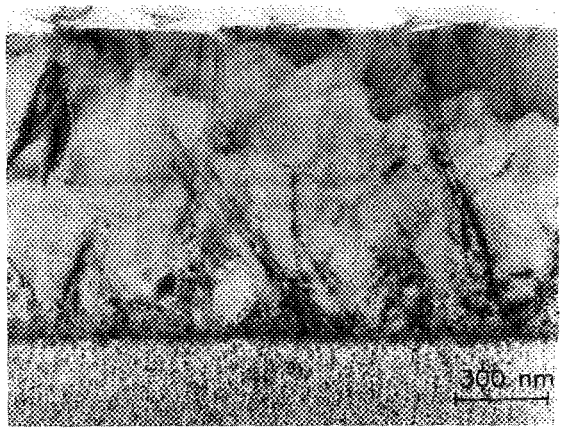

FIG. 3. Lattice-image TEM of GaAs/porous Si interface (aligned substrate). GaAs is shown to penetrate into the pores.

III. RESULTS AND DISCUSSION

Surface morphologies of the GaAs on porous Si and GaAs on Si layers are found to be generally similar and smooth although some features are found with a density of 2×10^8 cm^{-2}. The roughness of the porous Si surface does not seem to deteriorate the surface morphology of the GaAs on porous Si samples when compared to that of the GaAs on Si samples grown at the same time.

The crystallinity of the GaAs layers is examined by Rutherford backscattering spectroscopy (RBS). As shown in Fig. 1, the minimum channeling yield x_m of the GaAs on porous Si is 10%, a little smaller than x_m of 16% for the GaAs on Si samples. Furthermore, the comparison of the dechanneling behaviors of Figs. 1(a) and 1(b) indicates that the crystallinity of GaAs grown on porous Si substrates improves more rapidly than GaAs on Si as the epitaxial GaAs thickness increases.

From cross-section TEM, the dominant defects in GaAs on porous Si layers are microtwins and stacking faults as shown in Fig. 2. Both microtwins and stacking faults originate from the GaAs/porous Si interface. The majority of microtwins terminate within the first 190 nm of the epitaxial layer and the defect density is reduced to 2×10^9 cm^{-2} at the GaAs surface. GaAs is observed to penetrate into the pores as in Fig. 3. The nucleation of GaAs in the pores is suspected to cause the formation of microtwins and stacking faults.

To eliminate the penetration of GaAs and to reduce the high density of microtwins and stacking faults, a 50-nm thickness of Si buffer layer is grown on the porous Si substrate. The Si buffer layer is shown to bridge over the pores and to smooth the surface of porous Si in Fig. 4. The defect structure of the GaAs layer grown on this Si buffer is shown in Fig. 5, where the dominant defects are threading dislocations instead of microtwins and stack faults. The difference of defect structures for GaAs grown on porous Si and on buffer layer–porous Si samples suggests that the surface roughness of porous Si indeed results in the formation of microtwins and stacking faults.

Samples are also grown on the tilted substrates with and without Si buffer layers. From TEM micrographs, no significant difference between the tilted and aligned substrates is

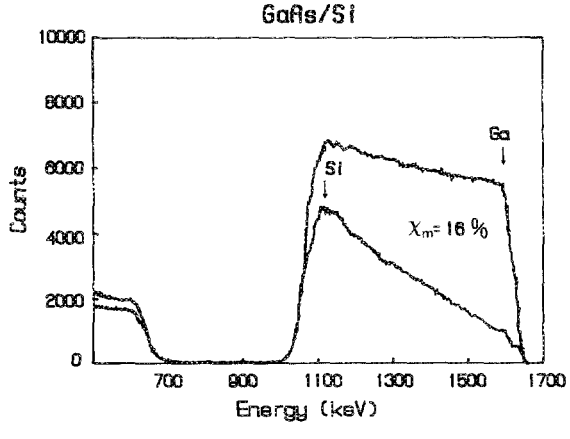

FIG. 2. Cross-section TEM of GaAs on porous Si (aligned substrate) showing that the dominant defects in GaAs layer are microtwins and stacking faults which originate from the GaAs/Si interface.

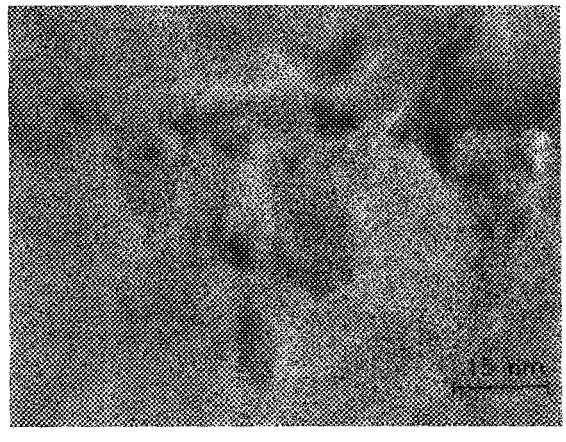

FIG. 4. Lattice-image TEM of GaAs/Si buffer/porous Si interface (aligned substrate). The Si buffer layer of 50-nm thickness has bridged over the pores. Microtwins and stacking faults are largely reduced and localized at the GaAs/Si buffer interface.

FIG. 5. Cross-section TEM of GaAs on Si buffer/porous Si (aligned substrate) showing the remaining large density of threading dislocations.

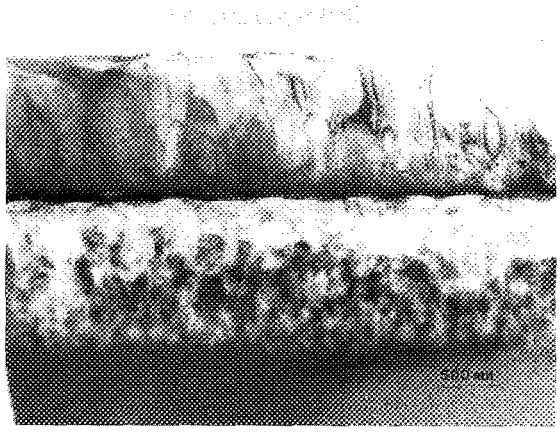

FIG. 6. Cross-section TEM of GaAs on Si buffer/porous Si (four tilted substrates). The defect structure and density are similar to those for aligned substrates as in Fig. 5.

observed in our present study. Figure 6 shows the TEM micrograph of the GaAs layer grown on the Si buffer layer on the tilted porous Si substrate. The defect structure and density are similar to those for aligned substrates.

To further reduce the defect density, several parameters have to be optimized. The growth conditions, porosity, and buffer layer thickness should be varied for examination of the effect of each parameter on grown GaAs epitaxial layers. Alternatively, a heterobuffer system such as GaAs/$Si_{1-x}Ge_x$/porous Si can be adopted. By tuning the Ge percentage of the buffer layer, defects may be confined in the heterobuffer layer.

IV. SUMMARY

GaAs layers have been grown on (100) aligned and tilted porous Si substrates and no significant difference of the qualities between them are observed. The GaAs growth is also done either directly on porous Si or on a thin Si buffer layer on porous Si. In the former, the dominant defects are found to be microtwins and stacking faults which originate from the roughness of porous Si surface. For the latter, the thin Si buffer layer of 50-nm thickness is shown to effectively smooth the porous Si surface and to reduce microtwins and stacking faults. There remains a high density of threading dislocations in the buffered samples. It is expected that the density may be reduced further by optimizing the growth conditions, porosity, and buffer layer thickness. Alternatively, a heterobuffer system such as GaAs/$Si_{1-x}Ge_x$/porous Si may also be used to further suppress the defect density of GaAs epitaxial layers.

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